

CLAIMS

1. A voltage regulator with quick response, comprising:
an output terminal, supplying a regulated voltage; and
a first boost circuit, which is controlled for alternately accumulating a first charge in a first operating condition and supplying said first charge to said output terminal in a second operating condition; wherein said first boost circuit comprises a compensation stage feeding said output terminal with a second charge substantially equal to said first charge when said first boost circuit is in said first operating condition.

2. The regulator according to claim 1 wherein said compensation stage comprises a controlled current-source circuit connected to said output terminal and supplying said second charge in said first operating condition.

3. The regulator according to claim 2 wherein said compensation stage comprises a current-sensor circuit, which is selectively connected to said output terminal in said first operating condition.

4. The regulator according to claim 3 wherein said controlled current-source circuit is controlled by said current-sensor circuit.

5. The regulator according to claim 4 wherein said current-sensor circuit is configured to be traversed by a first current absorbed by said first boost circuit in said first operating condition and in that said controlled current-source circuit is controlled so as to supply to said output terminal a second current equal to said first current.

6. The regulator according to claim 4 wherein said current-sensor circuit and said controlled current-source circuit comprise a first and, respectively, a second current-mirror circuit cascade-connected.

7. The regulator according to claim 6 wherein said current-sensor circuit and said controlled current-source circuit have a reciprocal mirroring ratio.

8. The regulator according to claim 7 wherein said first boost circuit has a control terminal receiving a control signal having a first logic value in said first operating condition, and a second logic value in said second operating condition.

9. The regulator according to claim 7 wherein said first boost circuit comprises a capacitive element.

10. The regulator according to claim 9 wherein said first boost circuit comprises a supply line, which supplies a supply voltage greater than said regulated voltage, and said capacitive element has a first terminal, selectively connected to a reference-potential line in said first operating condition, and to said supply line in said second operating condition; and a second terminal connected to said output terminal.

11. The regulator according to claim 9 wherein said current-sensor circuit comprises a first current-mirror transistor and a second current-mirror transistor, which have gate terminals connected to each other and respective source terminals connected to said reference-potential line, said first current-mirror transistor having a drain terminal connected to said gate terminals and being selectively connected to said first terminal of said capacitive element in said first operating condition.

12. The regulator according to claim 11 wherein said controlled current-source circuit comprises a third current-mirror transistor and a fourth current-mirror

transistor, which have gate terminals connected to each other and source terminals connected to said supply line, said third current-mirror transistor having a drain terminal connected to said gate terminals and said fourth current-mirror transistor having a drain terminal connected to said output terminal.

13. The regulator according to claim 11 wherein said first boost circuit comprises a drive stage having a first supply terminal connected to said supply line and a second supply terminal connected to the drain terminal of said first current-mirror transistor; an input forming said control terminal; and an output selectively connected to said first supply terminal in said second operating condition, and to said second supply terminal in said first operating condition.

14. The regulator according to claim 13 wherein said first terminal of said capacitive element is connected to said output of said drive stage.

15. The regulator according to claim 1, further comprising a second boost circuit connected in parallel to said first boost circuit.

16. The regulator according to claim 15 wherein said first and second boost circuits have the same structure and are controlled in phase opposition.

17. The regulator according to claim 15, further comprising a timing circuit associated with said first boost circuit and said second boost circuit and supplying respective drive signals in phase opposition to each other.

18. A regulated electronic device, comprising:
a load circuit; and
a voltage regulator supplying a regulated voltage, and be selectively connected to the load circuit, said voltage regulator including:

an output terminal, supplying a regulated voltage; and

a first boost circuit, which is controlled for alternately accumulating a first charge in a first operating condition and supplying said first charge to said output terminal in a second operating condition; wherein said first boost circuit comprises a compensation stage feeding said output terminal with a second charge substantially equal to said first charge when said first boost circuit is in said first operating condition. 19. The device according to claim 18, further comprising control unit connected to said voltage regulator to control said first boost circuit in said first operating condition when said load circuit is disconnected from said voltage regulator and in said second operating condition when said load circuit is connected to said voltage regulator.

20. The device according to claim 18 or 19 wherein said load circuit is a non-volatile memory array and said regulated voltage is a read/write voltage.

21. A method for regulating a voltage on a terminal selectively connected to a load, comprising the steps of:
accumulating a first charge, when said terminal is disconnected from said load; and
injecting said first charge into said terminal, when said terminal is connected to said load;
wherein said step of accumulating comprises supplying said terminal with a second charge equal to said first charge.

22. The method according to claim 21 wherein said step of accumulating comprises absorbing a first current from said terminal.

23. The method according to claim 22 further comprising the step of measuring said first current.

24. The method according to claim 22 wherein said step of supplying a second charge comprises supplying a second current equal to said first current.

25. The method according to claim 24 wherein said step of supplying a second current comprises mirroring said first current.

26. The method according to claim 21 wherein said step of supplying said second charge comprises taking said second charge from a supply line arranged at a supply voltage higher than said voltage on said terminal.

27. A regulating electronic device, comprising:
a load;
a regulating terminal selectively connected to the load;
means for accumulating a first charge, when the terminal is disconnected from the load; and
means for injecting the first charge into the terminal, when the terminal is connected to the load;
wherein the accumulating means includes means for supplying the terminal with a second charge equal to the first charge when the terminal is disconnected from the load.

28. The device of claim 27 wherein the accumulating means absorbs a first current from the terminal.

29. The device of claim 28 wherein the supplying means supplies to the terminal a second current equal to the first current.

30. The device of claim 28 wherein the supplying means include a first current mirror that mirrors the first current to produce a second current that the supplying means supplies to the terminal.

31. The device of claim 28, wherein the supplying means include:
a first current mirror that mirrors the first current to produce a second current, the first current mirror having a mirror ratio of $N:1$; and
a second current mirror that mirrors the second current to produce a third current, the second current mirror having a mirror ratio of $1:N$ and supplying the third current to the terminal when the terminal is disconnected from the load.